

I hereby certify that this correspondence is being deposited by FACSIMILE to the Commissioner of Patents and Trademarks, Washington, DC on November 14, 2002 by Colleen Dew.

Colleen J. Dew

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2822

In re application of : November 14, 2002  
Axel Brintzinger et al. : Examiner: Monica Lewis  
Serial No. : 09/873,537 :  
Filed: June 4, 2001 : IBM Corporation  
Title: DUAL DAMASCENE ANTI-FUSE : Dept. 18G/Bldg, 300-482  
WITH VIA BEFORE WIRE : 2070 Route 52  
Hopewell Junction, NY  
12533-6531

Request for Reconsideration

**FAX RECEIVED**

Commissioner for Patents and Trademarks  
Washington, D.C. 20231

NOV 14 2002

TECHNOLOGY CENTER 2800

Sir:

The following request for reconsideration is submitted in response to the office action dated August 14, 2002.

The invention centers on novel interconnect structures having an anti-fuse formed as a layer having openings that define via locations. The structures of the invention advantageously incorporate anti-fuses at reduced manufacturing cost.

Boardman et al. (US 5120679) discloses a structure where the vias are defined by holes in thick dielectric layer 46. The antifuse layer 52 is removed from all locations except for holes where the antifuses are desired. See Figures 3c-3f. Boardman et al. does not disclose or suggest an anti-fuse layer with an

opening which defines a via location.

Chang (US 5565703) discloses an antifuse structure where a dielectric layer 37) is deposited over the periphery of an antifuse layer 36 to define a location of a conductive plug 50. Chang does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

Go et al. (US 5592016) discloses anti-fuse structures which are located above or below vias. Go et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

McCollum et al. (US 5770885) discloses a silicon oxynitride layer on a substrate over which an amorphous silicon anti-fuse is formed. McCollum et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

For the above reasons, applicants submit that the present claims are patentable over the prior art of record and that the application is in condition for allowance. Such allowance is earnestly and respectfully solicited.

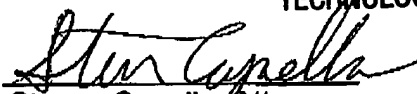
**FAX RECEIVED**

Respectfully submitted,  
Axel Brintzinger et al.

NOV 14 2002

TECHNOLOGY CENTER 2800

By



Steven Capella, Attorney  
Reg. No. 33,086  
Telephone: 845-894-3669

